### Objective

-To become familiar with the input/output characteristics of several types of standard flip-flop devices and the conversion among them.

### References

- Donald P. Leach: *Experimental in Digital Principles, 3\textsuperscript{rd} Edition*
- Malvino/Leach: *Digital Principles and Applications*
- Bartee: *Digital Computer Fundamentals, 6\textsuperscript{th} Edition*
- John F. Wakerley: *Digital Designs, Principle and Practice, 2\textsuperscript{nd} Edition*
- Ronald A Reis: *Digital Electronics Through Project Analysis, 1\textsuperscript{st} Edition*

### Component

- 1-74LS00 TTL IC
- 1-74LS74 TTL IC
- 1-74LS76 TTL IC

### Introduction

Logic circuit whose outputs depend upon circuit inputs as well as previous values of circuit outputs described as their present states are known as sequential logic circuits. A sequential system can be defined in terms of its inputs and present state. That is, the next state of the sequential system can be determined from these two quantities.

The (clocked) RS, D, JK and T flip-flops are characterized by the following state tables.
The “?” in the RS flip-flop state table (refer to table 1) means that when R = 1 and S = 1 then the next state is not determined explicitly.

**Procedure**

1) Construct the cross-coupled NAND gate basic RS flip-flop depicted in fig 6.1 and verify its sequential operation by completing the timing diagram shown in fig 6.2.
2) Construct the clocked RS flip flop of fig 3. Complete timing diagram as in fig 6.2 but add clock pulses as extra input. Use pulse switch as your clock source.

3) Simultaneously application of ones to R and S of the clocked RS flip flop, observe the outputs.

4) Since the constructed clocked RS flip flop is symmetric, we can change the position of R & S, and Q and Q’. It is still a clocked RS flip flop. Repeat step 3, see what has happened. Give your conclusion.
5) Using the 74LS74 dual D flip flop, investigate the operation of the D flip-flop (see fig 6.4). Compare your result with the state table given above. Pay attention to the change in state of the device as the clock signal is rising or falling. Compare the following timing diagram.

![D Flip Flop Diagram](image)

**Fig 6.4 : D Flip Flop**

Assume when $t=0$, $Q=0$

![Timing Diagram](image)

**Fig 6.5 : Timing Diagram**

6) Let input R open, ground the input S, watch the output and then let S open, ground R, watch the output. Determine the usage of R and S.
7) Using the 74LS76 dual JK flip flop, determine its logical operation. The circuit diagram is shown in fig 6.6. Pay attention to the change in state of the device as the clock signal is rising or falling. Compare the following timing diagram.

Fig 6.6 : JK Flip flop

assume when t=0, y=0

Fig 6.7 : Timing diagram
8) The flip flop can simulate each other. Construct the circuit shown in fig 6.8. Verify its sequential operation as a D flip flop. Complete the following timing diagram. Compare it with the timing diagram of fig 6.5.

![Fig 6.8: D flip flop (constructed by JK FF)](image)

**Fig 6.8: D flip flop (constructed by JK FF)**

**Fig 6.9: Timing Diagram**

Assume when t=0, Q=0
9) Wire the circuit shown in fig 6.10, verify that it is a T flip flop by drawing the timing diagram for the T flip flop.

**Fig 6.10 : T flip flop**
Objectives

- To design a ripple counter using JK flip flop.
- To connect a pre-settable counter and observe its operation.
- To create different counter module by decoding outputs and loading preset inputs.

Introduction

A counter is a circuit consisting of a number of Flip Flop and gates working together to count the number of clock pulses applied to its input. Such counters are used in digital clocks, frequency counters, digital voltmeters, digital computers, and numerous other applications. There are numerous types of counters, and we cannot look at theme in this experiment. The basic binary counter is probably the simplest to construct and form the basis for more advanced types of counters. In this experiment, we look at some of the counter circuits found most often and give you an opportunity to connect and observe them.

Ripple Counter (Asynchronous)

A ripple counter is a serial counter. The clock input is applied to only the first of the series of the Flip Flop. Clock pulses for the other Flip Flop come from the preceding Flip Flop. Thus, the clock pulse “ripple” through the circuit in a series fashion. Such circuit is also called asynchronous since the only pulse required for the operation is the clock pulse.

The JK Flip Flop have the J and K inputs both tied high, which allows them to toggle with each input pulse. Fig 7-1 shows a 4-bit ripple counter.
Synchronous Counters

The synchronous counter has the limitation of the time lag in triggering all the Flip Flop. To cure this problem, parallel counters can be used. The logic diagram for a 3-bit parallel counter is shown in fig 7.2. Note that all CLK inputs are tied directly to input clock. They are wired in parallel. Note that also the use of the AND gate at the output of Flip Flop 2 which will either hold Flip Flop 3(AND=0), or toggle Flip Flop 3(AND=1).
UP DOWN IC Counter: The 74193

The 74193 is a synchronous up-down 4-bit binary counter. It has a master reset (CLR), and it can be reset to any desired count with the parallel load inputs. Basically, it functions like any binary counter, except that it has two clock inputs, one for UP counting, and the other for DOWN counting. The logic symbol for the 74193 is shown in fig 7-3 (examine the data sheet). **LOAD** is a control input to load data into pins A, B, C and D.

![Logic Symbol](image)

**Figure 7.3**

Pin CLR is the master reset, and it is normally held below (a high level on CLR will reset all FF).

**CO** and **BO** are outputs to be used to drive the following 74193’s and we shall simply leave them open. The clock inputs are UP and DOWN. Placing the clock on UP will cause the counter to count UP, and placing the clock on DOWN will cause the counter to count DOWN. Note that the clock should be connected to either UP or DOWN, but not both, and the unused inputs should be held HIGH. The outputs of the counter are QA, QB, QC and QD.

**Components needed:**

1. 74LS00 Quad NAND Gate TTL IC
2. 74LS76 Dual JK Flip Flop
3. 74LS93 4 bit binary counter
4. 74LS193 4 bit UP-DOWN counter
5. Oscilloscope
Procedure

1) Construct the Ripple counter shown in fig 7.1. Clear all output FF by giving a negative clock pulses to the clear inputs, and apply the clock of a one shot actuated by the push button. Repeat that for 17 clock pulses. Record the output QA, QB, QC and QD of the counter in table 1 below

\( \text{MSB} = QD ; \text{LSB} = QA \)

Draw the timing diagram of the above circuit.

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Table 1

2) Use the 74LS93 counter to implement

a) A modulo 16 counter;

b) A decade counter

3) Make these connections to the counter of fig 7.3

- Pin 15, 1, 10 and 9 (preset data inputs) Open
- Pins 12 and 13 (CO and BO) Open
- Pins 3, 2, 6 and 7 (outputs) to LED’s
- Pin 11 (LOAD) to +Vcc
- Pin 16 (+Vcc) to +Vcc
- Pin 14 (CLR) to ground
- Pin 8 (GND) to ground
4) For the count-up mode, connect pin 4 (DOWN) to +Vcc, and apply the clock to pin 5(UP). Record carefully the 4 output waveforms with respect to the clock.

5) For the count-down mode, connect pin 5(UP) to +Vcc, and apply the clock to pin 4(DOWN). Record the resulting output waveforms.
A flip-flop is a sequential device able to store one binary bit of information. More general sequential device, constructed by interconnecting a number of flip—flops, can process one or more bits of information and are known as REGISTERS and COUNTERS.

A REGISTER is a memory device used for storing and manipulating data registers (found by the thousand in digital computers) may be classified according to how their stored information is entered or removed. A SERIAL register is one in which the data is entered or removed one bit at a time and a PARALLEL register accepts or transfers all bits of data simultaneously. Serial input – parallel output networks as well as the inverse are also available.

References

Donald P. Leach: Experimental in Digital Principles, 3rd Edition

Component

1-74LS04 Hex inverter TTL IC
3-74LS95 4 bit parallel access shift register
2-74LS74 Dual D FF TTL IC
1-74LS193 4 bit UP-DOWN counter
**Procedure**

A) Four-bit Memory Register (Parallel In-Parallel Out)

Memory register typically provide temporary storage of data, such as the count from a counter. The device supplying the data is then free to perform other tasks while the data is preserved for the future use, such as being decoded and read out or being displayed.

Install two 74LS74 Dual D type Positive Edge Trigger Flip-Flop IC’s into the logic lab breadboard. Connect these D flip-flops to implement the following Parallel In-Parallel Out 4 Bit memory register shown in fig 8-1. Use switches as inputs and LED's for outputs. Also, remember the power connections for each chip.

Before entering any data, be sure to clear all flip-flops. Remember that the clear should be normally be in the HIGH state. Switch the clear input as follows: HIGH→LOW→HIGH to clear the Flip-Flop. Describe the operation of this circuit as a 4-bit memory devices by entering various combinations of inputs (A,B,C,D) and observing the outputs (Q1,Q2, Q3,Q4) as you will simulate clock pulses on the CLK bus (i.e common clock input to all the flip-flops ). What range of numerical values can be stored in this 4-bit memory register? Show a sample timing diagram for two different sets of input data.

![Figure 8.1](image-url)
B) Four-bit Shift Register with Serial Entry

Another type of register is a shift register. Although it can also stored data as a memory register, it is more often used to process or move the data. Usually the movement is a shift of data from one stage of the register to an adjacent stages either from left to right (a right shift register), from right to left (a left shift register) or in both directions (a bit-directional shift register). Shift registers differ from memory registers in that adjacent stages are connected to allow shifts of data from one stage to the next.

A serial entry of shift register capable of storing 4-bit words as shown in fig 8.2. The stages used here are D flip-flop, but other types may used as well. The outputs Q1, Q2, Q3 and Q4 are made O initially by a Clear control. The first data bit, say D1 is applied to the serial input terminal; and on the first positive edge of the CLK, it is loaded into the first stage as Q1 = D1. Next D2 is applied and clocked in as Q1 = D2, at which point D1 is shifted to Q2 = D1. Continuing the process with D3 and D4, the next two serial entries, we have Q1 = D4, Q2 = D3, Q3 = D2, Q4 = D1.

Try several input combinations for this sequential network to learn how it operates. Observe that the input data may be taken in either a serial or parallel manner. That is, the outputs Q1, Q2, Q3 and Q4 may be all read simultaneously or the output may be read one bit at a time at the output Q4 of the fourth stage. Determine the timing diagram for the following set of inputs; D1 = D4 = 1, D2 = D3 = 0. Show the input CLK, Q1, Q2, Q3 and Q4.

Carefully observe the time delay on the oscilloscope and explain how this happens.

Figure 8.2
Pin Connection Diagram

74LS00 TTL IC

74LS74 TTL IC
74LS76 Dual JK Flip Flop

74LS193 4 bit UP-DOWN counter
74LS93 4 bit binary counter

74LS95 4 bit parallel access shift register