ECOM 4101: COMMUNICATIONS ENGINEERING LAB II

SEMESTER 1, 2023 / 2024

EXPERIMENT NO. 4

PSK Modulation

NAME: ___________________________________ MATRIC NO: __________________

DATE: ___________________________ SECTION: ___________________________
**PSK MODULATION**

**Objectives**
- To describe the PSK modulation and demodulation
- To carry out a PSK connection, with absolute modulation
- To examine the noise effect on the connection

**Material**
- Power unit PSU
- Module holder base
- Individual Control Unit SIS1
- Experiment module MCM31
- Oscilloscope

**THEORETICAL NOTIONS**

**Phase Shift Keying - PSK**
In this kind of modulation, the sine carrier takes 2 or more phase values, directly determined by the binary data signal (2-phase modulation) or by the combination of a certain number of bits of the same data signal (N-phase modulation).

In 2-phase PSK modulation, called 2-PSK, or Binary PSK (BPSK), or Phase Reversal Keying (PRK), the sine carrier takes 2 phase values, determined by the binary data signal (fig.1). A modulation technique is the one using a balanced modulator. The output sine-wave of the modulator is the direct or inverted (i.e. shifted of 180°) input carrier, as function of the data signal.

**Constellation Diagram**
The modulation states of the PSK Modulator are represented with points in a vectorial diagram. Each point is a modulation state, characterized by a phase and an amplitude. This representation is called *constellation diagram*, or more simply *constellation*.

**Main aspects**
The main aspects characterizing the 2-PSK are:
- use of digital radio transmission
- it requires circuits of average-high complexity
- high possibility of error but lower than the FSK
- if $F_b$ is the bit transmission speed, the minimum spectrum $B_w$ of the modulated signal is higher than $F_b$
- the transmission efficiency, defined as the ratio $F_b$ and $B_w$, is lower than 1
- the *Baud* or *Baud rate*, defined as the Modulation speed or symbol speed, is equal to the transmission speed $F_b$. 
2-PSK Modulator

The block diagram of the 2-PSK modulator is shown in fig.2. The sine carrier (1200 Hz) is applied to an input of the balanced modulator 1; a data signal (indicated with I) is applied to the other input. The circuit operates as balanced modulator, and multiplies the two signals applied to the inputs. Across the output, the sine carrier is direct when the data signal is to low level (bit "0"), inverted (shifted 180°) when the bit is "1". The 2-PSK signal then enters the adder, used for FSK/QPSK/QAM modulations, and exits via a separator stage. The 6dB attenuator makes the signal amplitude half, and is activated only by the QAM. To block the operation of the balanced modulator 2 in 2-PSK mode, the data input of the modulator 2 must be set to J3=b.

![Figure 1: 2-PSK Modulation](image1)

![Figure 2: 2-PSK Modulator mounted on the module](image2)

2-PSK Demodulation with Carrier Regenerator

The demodulation (fig.3) is carried out via a product demodulator, which is reached by the PSK signal and a locally regenerated carrier. This must have the same frequency and phase of the one used in transmission (it must be coherent with the received signal), and is taken from the PSK signal as described further on.

Mathematically, the demodulation process is developed as follows. Consider:

- \(+\sin(w_c \cdot t)\) = instant PSK signal corresponding to the data bit "1", with \(f_c = \frac{w_c}{2 \pi}\) carrier frequency
- \(-\sin(w_c \cdot t)\) = PSK signal corresponding to the bit "0"
- \(\sin(w_c \cdot t)\) = regenerated carrier.
When the PSK signal is $\sin(w_c \cdot t)$ the demodulator supplies:

$[\sin(w_c \cdot t)] \cdot [\sin(w_c \cdot t)] = \sin^2(w_c \cdot t) = \frac{1}{2} \cdot [1 - \cos(2w_c \cdot t)] = \frac{1}{2} - \frac{1}{2} \cdot \cos(2w_c \cdot t)$

and contains a d.c. component $(\frac{1}{2})$ and an a.c. component with double frequency than the carrier $[\cos(2w_c \cdot t)]$. The alternate component can be removed with the low pass filter, and a positive voltage remains which represents the bit "1".

When the PSK signal is $-\sin(w_c \cdot t)$ the demodulator supplies:

$[-\sin(w_c \cdot t)] \cdot [\sin(w_c \cdot t)] = -\sin^2(w_c \cdot t) = \frac{1}{2} \cdot [1 - \cos(2w_c \cdot t)] = \frac{1}{2} + \frac{1}{2} \cdot \cos(2w_c \cdot t)$

The a.c. component is removed and a negative voltage remains which represents the bit "0".

**Carrier regenerator with quadratic law**

The carrier regenerator circuit must extract a signal _coherent_ (same frequency and phase) with the carrier from the PSK signal. A method used is the one of fig.3:

- a squarer circuit removes the $180^\circ$ phase shifts in the modulated carrier, to facilitate the same carrier regeneration by the next PLL circuit
- the PLL circuit generates a square-wave signal with double frequency than the PSK carrier
- a phase shifter circuit enables to properly adjust the phase of the regenerated carrier
- a frequency divider divides by 2 the square-wave supplied by the PLL, and provides the regenerated carrier in this way.

**Demodulator circuit**

The block diagram of the 2-PSK demodulator with coherent detector is shown in fig.4. It includes the following circuits:

- the carrier regenerator, which supplies a signal coherent (same frequency and phase) with the carrier of the PSK signal. It consists of:
  - a double squarer, which purpose is to remove the $180^\circ$ phase shifts in the modulated carrier, to facilitate the same carrier regeneration by the next PLL circuit
  - a PLL circuit, which generates a square-wave signal with frequency four times the one of the PSK carrier
  - a frequency divider by 4, to obtain the regenerated carrier. The double squarer and the frequency divider by 4 enables the use of the same circuit for carrier regeneration in the 4-PSK systems too.
- The 2-PSK demodulator (shown in the diagram as DEM I), consists in a double sampler. If the regenerated carrier phase is correct, the sampler output will contain only positive half-waves when the 2-PSK signal has a certain phase, only negative half-waves when the phase is reversed
- a low pass filter
- a squarer circuit (with output in TP29 in case of asynchronous data, which are not re-timed)
- a clock extraction and data re-timing circuit, in case of synchronous data (data output on TP31, clock on TP33).

The filter, the clock extraction and the data re-timing circuit are used to demodulate other kinds of signals, too.
Figure 3: 2-PSK Demodulation with carrier regenerator with quadratic law

Figure 4: 2-PSK Demodulator mounted on the module
PROCEDURE

Wave-forms of the 2-PSK Modulator

• MCM31 – Disconnect all jumpers
• SIS1 – Turn OFF all switches
• Power the module
• Set the circuit in 2-PSK mode, with 24-bit data source and without data coding (connect J1c-J3b-J4-J5-J6c, set SW2 = Normal, SW3 = 24 bit, SW4 = 1200, SW=PSK, SW7 = Squaring Loop, SW8 = BIT, ATT = min, NOISE = min.
• set an alternated data sequence 00/11 and push START
• connect the oscilloscope to TP6 and TP16 and examine the data signal and the 2-PSK signal. Adjust the phase (PHASE) to invert the phase of the carrier in correspondence to 0°.

Q1 Examine the carrier at the input TP12 and the output (TP 16) of the modulator. What can you note?

SKETCH THE GRAPHS FROM THE OSCILLOSCOPE:
Wave-forms of the 2_PSK demodulator

- Keep the last conditions (connect J1c-J3b-J4-J5-J6c, set SW2 = Normal, SW3=24 bit, SW4 = 1200, SW=PSK, SW7 = Squaring Loop, SW8 = BIT, ATT = min, NOISE = min.
- set an alternated data sequence **00/11** and push **START**
- connect the oscilloscope to TP16 and TP20, to examine the PSK signal before and after the communication Channel (Fig. 5)
- observe the affect of the communication channel on the PSK signal. As the communication channel is limited band, the phase transitions of the output PSK signal are slightly beveled.
- The PSK demodulator (indicated on the diagram as I DEM), consists in a double sampler, which samples the negative and positive half-wave of the incoming PSK signal. The sampling clock consists in the carrier regenerated by the Carrier Recovery Section
- Across TP21 you can note a rectangular signal which samples the negative half-wave of the PSK signal. The frequency of the sampling signal is equal to the frequency of the PSK carrier (1200 Hz), the sampling duration is equal to ¼ the period.

Q2 What kind of signal can you observe on the demodulator output (TP23)?

- The signal supplied by the PSK demodulator passes a low filter, which eliminates the residuals of the 1200 Hz carrier. Across the filter’s output (TP24, Fig. 5) you get the wave-form of the detected data signal.
- It can happen that the received signals are inverted in respect to the transmitted one. This can be understood as the demodulator does not know which of the coming phases is $0^\circ$ or $180^\circ$, and this ambiguity can take to the inversion of the demodulated data. The ambiguity is overcome by carrying out a data differential coding before the modulation. In case push Phase Sync to obtain data with proper sign.
- The squared data signal can be detected across TP31. See on the oscilloscope the correspondence between the transmitted data (TP6) and the received ones (TP31)
- Across TP32 see the reception clock (rectangular wave at 600 Hz), reconstructed starting from the data signal and used to re-time the same data.

![Figure 5: 2-PSK Waveforms](image_url)

- **SIS1** - *Turn ON switch S24*

**Q3** The data received on TP29 is not correct. Why?
SKETCH THE GRAPHS FROM THE OSCILLOSCOPE:

• SIS1 - Turn OFF switch S24
• Set now a data sequence with few alternation, e.g. all “1” and a single “0”, and push **START**
• Examine the signal across TP4 (transmitted data), TP31 (received data), TP32 (reception clock).
  Eventually push *Phase Sync* to obtain the data with proper sign across TP31.
• It can happen that the reception clock (TP32) is not stable, and that the received data (TP31) has some
  time different from the transmitted (TP4). This is due to a bad operation of the PLL which regenerates the
  reception clock.

**Q4 What can you observed at TP4, TP31 and TP32?**

• The Manchester coding of the data to be transmitted ensures there are always alternates in the transmitted
  signal, facilitating in this way the clock extraction by the PLL.
• Supply the 2-PSK modulator with the Manchester coded data (disconnect J1c and connect J1-d)
• The Received Data and the Reception Clock are now available after the Manchester coder (TP9 and TP10)
• Keep the same data sequence of the last case and see that:
  - The clock is now regenerated properly
  - The received data is equal to the transmitted ones

**Q5 What can you observed at TP4, TP9, TP3 and TP10?**